Instructor: Amir Alimohammad, Assistant Professor  
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Office: Fourth floor, Engineering, 403-E  
Office Hours: Tuesdays and Thursdays 12:30 PM – 1:45 PM. Feel free to make an appointment by email if you are not available during these hours.  
Class Schedule: Tuesdays and Thursdays 5:30 PM – 6:45 PM  
Class Location: GMCS– 306  
Class Website: Available on Blackboard  
Catalog Description: Not available (3 credits)  
Prerequisite Course: CompE 572

Course Description: This course focuses on the principles and practices involved in the design of high-performance and low-power application-specific integrated circuit (ASIC) chips. This course will offer valuable design experience through design projects and will provide deeper insight into efficient future large-scale chip designs.

Topics Covered
1. Simulation of static and dynamic circuit families, including CMOS, DCVSL, CPL, TG, domino logic (DL), MODL, compound DL in Cadence  
2. Static and dynamic latches and flip-flops  
3. Transistor-level datapath design and verification using Verilog hardware description language  
4. Method of logical effort  
5. Timing analysis of register-based and latch-based designs  
6. Replacement of flip-flops by latches in ASICs  
7. Avoiding races with latches  
8. Reducing the timing overhead  
9. Slack passing and time borrowing with latches  
10. Optimal latch positions with two clock phases  
11. ASIC performance improvement using useful-skew clock synthesis  
12. Power consumption and low power design methodologies

Course Objectives
1. Gain knowledge about various ratioed and ratio-less static circuit families, including CMOS, pseudo-nMOS, differential cascode voltage switch logic, pass transistor logic, complementary pass transistor logic, and transmission gate logic.  
2. Gain knowledge about various dynamic circuit families, including domino logic, dual-rail domino logic, multiple-output domino logic, compound domino, and np-domino.  
3. Being able to model, debug and simulate static and dynamic digital circuits using CAD tools.  
4. Able to utilize various static and dynamic latches and flip-flops in digital circuits.  
5. Able to describe digital circuits at the transistor level using Verilog hardware description language, simulate, and verify it.  
6. Understand the method of logical effort.  
7. Learn about datapath subsystem design, including arithmetic modules, comparators, counters, LFSRs  
8. Learning about dynamic and static memories.
9. Learning about skew-tolerant design methodology.

10. Understand timing analysis of register-based and latch-based designs.

11. Understand various sources of energy dissipation in digital circuits and approximate power consumption.

Course Grading

- Homework assignments **15%**
- Quizzes **20%**
- Project **25%**
- Final exam **40%**

Course Materials

- Lecture slides, class notes, academic articles, book chapters, web pages, industrial documentation and manuals, homework assignments, and quizzes.
- Handouts will be posted on the class webpage. Check the class webpage regularly for updates.
- Recommended textbooks (optional)

Course Policies

1. Attending the classes is not mandatory; however, if you are absent, it is your responsibility to know the announcements made in class and material covered. Generally announcements will be given in class and/or via Blackboard.

2. Audio or video recording devices are not permitted.

3. If you have missed the class and/or office hours and have questions about lectures or homework assignments, please post your technical questions on the "discussion board" on Blackboard. Other students may be having the same questions as you. This allows other students to engage in the discussion as well. I give extra credits to those who are most active on the discussion board.

4. You must meet the deadline for your assignments and projects and take the exam/quiz at the announced date and time. Deadlines are not subject to change and no late assignments/projects are accepted.

5. If you cannot meet the deadline for a valid reason, such as hospitalization, I require supporting documents to prove your reason and you should provide them to me before the date of your exam/assignment/project.

6. If your reason is accepted, then you will be given a make-up exam. Note that the make-up exam can be more difficult than the scheduled exam. I cannot give you the exact same exam.

7. You must bring any issues regarding your exams or assignments to my attention within a week. No changes will be made after this time period.

8. You have only one week to submit a written request along with your original assignment/exam for re-grading. All submissions are re-graded in their entirety.
9. Homework papers are due at the beginning of class
10. Quizzes are given at the end of the lecture.
11. The final exam covers all topics.
12. Your final grade is based on the homework assignments, quizzes, exams, and your project. No extra credit options, such as projects, assignments, etc. are available. This is not fair to other students.
13. Final grade will be calculated SOLELY based on the above percentages. Grading percentage is NOT subject to change.
14. All the exams (quizzes and final exam) are closed book/note.
15. I allocate the beginning of every lecture to your questions. Please ask your technical questions in class instead of via email. You can come to my office during office hours or post your questions on the discussion board if you don't want to ask them in class.

Important Dates

<table>
<thead>
<tr>
<th>Date</th>
<th>Event</th>
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<tbody>
<tr>
<td>August 26</td>
<td>First day of classes</td>
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<tr>
<td>September 2</td>
<td>Holiday – Labor Day. Faculty/staff holiday. Campus closed</td>
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<tr>
<td>September 5</td>
<td>Last day for faculty to drop students from classes</td>
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<tr>
<td>October 30</td>
<td>Last day to officially withdraw from all classes for Fall 2012</td>
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<tr>
<td>November 11</td>
<td>Holiday – Veteran’s Day observed. Faculty/staff holiday. Campus closed</td>
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<tr>
<td>November 28-29</td>
<td>Holiday – Thanksgiving recess. Faculty/staff holiday. Campus closed</td>
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<tr>
<td>December 11</td>
<td>Last day of classes before final examinations</td>
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<td>December 12</td>
<td>15:30 PM to 17:30 PM Final Exam</td>
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10 Tips on how to get a good grade

1. Attend lectures and ask questions, offer comments, stay involved
2. The lecture material is NOT the most challenging part of the course
3. You should be able to understand everything as we go along. Do not fall behind in the lectures
4. You need to understand the material well enough to apply it in new situations
5. Spend 2-4 hours with the materials outside of class time for each hour in class
6. Notes will be posted online before the lecture (usually the night before). Look at them before
class

7. Come to office hours

8. The exams will test your depth of knowledge. You need to understand the material well enough to apply it in new situations


10. Be clear. Formulate the problem, your solution, and your results clearly. Compare your results with published results