Instructor: Dr. Amir Alimohammad, Associate Professor
E-Mail: aalimohammad@mail.sdsu.edu

Office Hours: Tuesdays and Thursdays 12:30 PM – 1:45 PM
Feel free to make an appointment by email if you are not available during these hours.

Office Location: Fourth floor, Engineering, 403-E

Class Schedule: Mondays and Wednesdays 2 PM – 3:15 PM

Class Location: GMCS-307

Class Website: Available on Blackboard (http://blackboard.sdsu.edu)

Prerequisite Course: CompE 572

Enrollment and Crashing Policy: All students must have enrolled in class and met the prerequisite. Crashing and auditing are not allowed.

Course Description

This course focuses on the principles and practices involved in the design of high-performance and low-power application-specific integrated circuit (ASIC) chips. This course aims to provide a strong foundation for graduate students to understand the principles and practices of designing application-specific integrated circuits using state-of-the-art computer-aided design tools. The course will offer valuable design experience through design projects and will provide deeper insights into future large-scale integrated circuit designs.

Topics Covered

1. Static and dynamic circuit families, including CMOS, DCVSL, CPL, TG, and domino logic
2. Method of logical effort
3. Static and dynamic latches and flip-flops
4. Replacement of flip-flops by latches in ASICS
5. Timing analysis of register-based and latch-based designs
6. Avoiding races with latches
7. Reducing the timing overhead
8. Slack passing and time borrowing with latches
9. Optimal latch positions with two clock phases
10. ASIC performance improvement using useful-skew clock synthesis
11. Power consumption and low power design methodologies

Course Objectives

1. Gain knowledge about various ratioed and ratio-less static circuit families, including CMOS, pseudo-nMOS, differential cascode voltage switch logic, pass transistor logic, complementary pass transistor logic, and transmission gate logic.
2. Gain knowledge about various dynamic circuit families, including domino logic, dual-rail domino logic, multiple-output domino logic, compound domino, and np-domino.
3. Understand the method of logical effort.
4. Able to utilize various static and dynamic latches and flip-flops in digital circuits.
5. Understand timing analysis of register-based and latch-based designs.
7. Understand various sources of energy dissipation in digital circuits and approximate power consumption.
Course Activities and Grading Policy

- Homework assignments 10%
- Quizzes 25%
- Midterm exam 25%
- Final exam 40%

- Assignments and quizzes are varied in scope and emphasis (e.g., size and grade-weighting).

Course Materials and Resources

- Lecture slides, class notes, academic articles, book chapters, web pages, industrial documentation and manuals, homework assignments, and quizzes.

- Course materials will be posted on the class webpage on BlackBoard. Various directories will be created to organize the course materials. Check the class webpage regularly for updates.

- Optional textbooks:
  - “CMOS VLSI Design” by N. Weste and D. Harris.
  - “Closing the Gap Between ASIC & Custom: Tools and Techniques for High-Performance ASIC Design” by D. Chinnery and K. Keutzer.
  - “Low-Power Digital VLSI Design: Circuits and Systems” by A. Bellaouar and M. Elmasry.

Students with Disabilities

If you are a student with a disability and believe you will need accommodations for this class, it is your responsibility to contact Student Disability Services at (619) 594-6473. To avoid any delays in the receipt of your accommodations, you should contact Student Disability Services as soon as possible. Please note that accommodations are not retroactive, and that I cannot provide accommodations based upon disability until I have received an accommodation letter from Student Disability Services. Your cooperation is appreciated.

Academic Honesty

As per 2012-2013 SDSU General Catalog (pages 466-480), San Diego State University expects the highest standards of academic honesty from all students. Violations of academic integrity including plagiarism, cheating, unauthorized collaboration on an exercise and/or exam, misappropriation of research materials, and any other forms of academic dishonesty that are intended to gain unfair academic advantage are not permitted. If your academic integrity is not maintained in an assignment or exam, you will automatically receive a grade of zero for that assignment or exam AND you will be reported to the Dean’s Office.