Instructor: Dr. Amir Alimohammad, Associate Professor
E-Mail: aalimohammad@mail.sdsu.edu

Office Hours: Tuesdays and Thursdays 12:30 PM – 1:45 PM
   Feel free to make an appointment by email if you are not available during these hours.

Office Location: Fourth floor, Engineering, 403-E
Class Schedule: Tuesdays and Thursdays 4 PM – 5:15 PM
Class Location: P-144
Class Website: Available on Blackboard (http://blackboard.sdsu.edu)

Prerequisite Course: CompE 270

Enrollment and Crashing Policy: All students must have enrolled in class and met the prerequisite. Crashing and auditing are not allowed.

Course Description
Design and verification of digital systems using Verilog hardware description language, commercially-available computer-aided design tools, and field-programmable gate arrays (FPGAs): datapath design, controller design, arithmetic units, memory design, testing and verification, FPGA architectures.

Topics Covered
1. Digital design methodologies and implementation strategies.
2. Numerical systems.
3. Datapath and controller design.
4. Arithmetic unit design.
5. Verilog hardware description language.
6. FPGA architecture.
7. Testing and verification of digital systems.

Learning Outcomes
1. Gain a deeper understanding of design methodologies and implementation strategies, such as programmable processors, reconfigurable logic, and custom designs.
2. Know about various numerical representations.
3. Demonstrate knowledge of various components of digital systems including datapath, such as arithmetic modules and register files, controllers, memory blocks, stack, and queue.
4. Being able to implement, debug, and simulate digital systems using a computer aided design tool.
5. Be familiar with architecture of FPGAs.
6. Understand testing of digital systems.

Course Activities and Grading Policy
- Homework assignments 10%
- Midterm exam 25%
- Final exam 40%
- Quizzes 25%

Assignments and quizzes are varied in scope and emphasis (e.g., size and grade-weighting).
Course Materials and Resources

- Lecture slides, class notes, academic articles, book chapters, web pages, industrial documentation and manuals, homework assignments, and quizzes.

- Course materials will be posted on the class webpage on BlackBoard. Various directories will be created to organize the course materials. Check the class webpage regularly for updates.

- Optional textbooks:
  - “The Verilog Hardware Description Language” by D. Thomas and P. Moorby.

- Online resources: There are plenty of online resources for Verilog HDL. You might find these useful:
  - http://www.sutherland-hdl.com/online_verilog_ref_guide/vlog_ref_top.html
  - http://verilog.renerta.com/

- You should review the textbook that you used in CompE 270.

- You should download the Xilinx ISE Webpack http://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.html

Students with Disabilities

If you are a student with a disability and believe you will need accommodations for this class, it is your responsibility to contact Student Disability Services at (619) 594-6473. To avoid any delays in the receipt of your accommodations, you should contact Student Disability Services as soon as possible. Please note that accommodations are not retroactive, and that I cannot provide accommodations based upon disability until I have received an accommodation letter from Student Disability Services. Your cooperation is appreciated.

Academic Honesty

As per 2012-2013 SDSU General Catalog (pages 466-480), San Diego State University expects the highest standards of academic honesty from all students. Violations of academic integrity including plagiarism, cheating, unauthorized collaboration on an exercise and/or exam, misappropriation of research materials, and any other forms of academic dishonesty that are intended to gain unfair academic advantage are not permitted. If your academic integrity is not maintained in an assignment or exam, you will automatically receive a grade of zero for that assignment or exam AND you will be reported to the Dean’s Office.