Instructor: Dr. Amir Alimohammad, Associate Professor

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Office Hours: Tuesdays and Thursdays 12:30 PM – 1:45 PM
Feel free to make an appointment by email if you are not available during these hours.

Office Location: Fourth floor, Engineering, 403-E

Class Schedule: Mondays and Wednesday 4 PM – 5:15 PM

Class Location: E-423

Class Website: Available on Blackboard (http://blackboard.sdsu.edu)

Prerequisite Course: CompE 375 and CompE 470

Enrollment and Crashing Policy: All students must have enrolled in class and met the prerequisite. Crashing and auditing are not allowed.

Course Description
The fundamentals and practice of modern processor design: Instruction set architecture, microarchitecture design, pipeline processors, data and control hazards, branch prediction, performance measurements, exception handling, out-of-order execution, multi-threading, context switching, memory hierarchy, parallelism, multi-core processors.

Topics Covered
1. Instruction set architecture
2. Microarchitecture design: Single-cycle, multi-cycle, and pipelined processor design
3. Handling data and control dependencies
4. Branch prediction
5. Out-of-order execution
6. Performance evaluation
7. Exception handling
8. Memory hierarchy and cache system
9. Data-level, instruction-level, thread-level parallelism
10. Multithreading and context switching
11. Multi-core processors and multiprocessors

Learning Outcomes
1. Understand the role of instruction set architecture.
2. Being able to design a single-cycle, a multi-cycle, and a pipelined MIPS-like processor in Verilog.
3. Learn about removing data and control dependencies.
4. Understand architectural techniques, such as branch prediction and register renaming.
5. Understand performance measurement techniques for a computing system.
6. Learn about exceptions and the process of handling exceptions.
7. Learn about superscalar processors and out-of-order executions.
8. Understand multithreading and context switching concepts.
9. Learn about memory hierarchy, cache system, and virtual memory.
10. Learn about various levels of parallelism, such as data-level, instruction-level, and thread-level.
11. Be familiar with multi-core and multiprocessor systems.
Course Activities and Grading Policy

- Homework assignments 10%
- Midterm exam 25%
- Quizzes 25%
- Final exam 40%

- Assignments and quizzes are varied in scope and emphasis (e.g., size and grade-weighting).

Course Materials and Resources

- Lecture slides, class notes, academic articles, book chapters, web pages, industrial documentation and manuals, homework assignments, and quizzes.
- Course materials will be posted on the class webpage on BlackBoard. Various directories will be created to organize the course materials. Check the class webpage regularly for updates.
- Optional textbooks:

Students with Disabilities

If you are a student with a disability and believe you will need accommodations for this class, it is your responsibility to contact Student Disability Services at (619) 594-6473. To avoid any delays in the receipt of your accommodations, you should contact Student Disability Services as soon as possible. Please note that accommodations are not retroactive, and that I cannot provide accommodations based upon disability until I have received an accommodation letter from Student Disability Services. Your cooperation is appreciated.

Academic Honesty

As per 2012-2013 SDSU General Catalog (pages 466-480), San Diego State University expects the highest standards of academic honesty from all students. Violations of academic integrity including plagiarism, cheating, unauthorized collaboration on an exercise and/or exam, misappropriation of research materials, and any other forms of academic dishonesty that are intended to gain unfair academic advantage are not permitted. If your academic integrity is not maintained in an assignment or exam, you will automatically receive a grade of zero for that assignment or exam AND you will be reported to the Dean’s Office.