EE 530 - SYLLABUS
Design & Analysis of Analog ICs

This course will cover the design and analysis of analog integrated circuit amplifiers. Much of the course will involve the extensive use of computer aided design tool such as SPICE (Simulation Program with Integrated Circuit Emphasis) programs. A solid background in circuits analysis and electronics is a necessary course pre-requisite (e.g., passing EE430 with “C” or better).

COURSE ADMINISTRATION AND OVERVIEW

Students will be divided into design teams of 2-3 each to work collaboratively on the design (using SPICE) of the input, gain, and output stages of an operational amplifier. Four reports of their work will be required throughout the semester. The first three will be a group effort while the fourth report will be done individually. Each member of the group will be expected to contribute equally to the overall effort and each member will be required to give a graded oral progress report by during the semester. Lectures, assigned reading, and homework problems will parallel the design project and present advanced topics beyond the project’s scope.

REQUIRED TEXTBOOK & RECOMMENDED REFERENCES


CLASS POLICIES

1. ATTENDANCE: Students are expected to attend all class sessions and thus will be held responsible for any lecture materials missed, quizzes missed, and all homework or SPICE assigned during absences. For examination class periods, absences due to non-compelling reasons will be result in a zero grade on that exam. THERE WILL BE NO MAKE-UP EXAMS!

2. LATE DROPS: As per the new campus policy, no drops permitted after the 3rd week of the semester.

3. ACADEMIC MISCONDUCT: Cheating on quizzes, midterms, SPICE assignments, or the final will be punished by a zero grade on that item and possibly also an automatic "F" for the course. Without exception, all incidences of academic misconduct will be reported to the Campus Judicial Coordinator for disciplinary action. Section 41301 of Title V of the California Code of Regulations defines academic misconduct as, “(a) Cheating or plagiarism in connection with an academic program at a campus.” Examples of cheating include using unauthorized notes or study guides during a test, unauthorized collaboration on design projects, stealing course materials, submitting falsified data, allowing one's work to be copied, copying another student's SPICE program/quiz/exam, using posted work from prior semesters, and intentionally assisting another individual in any of the above.

4. If you are a STUDENT WITH A DISABILITY and believe you will need accommodations for this class, it is your responsibility to contact Student Disability Services at (619) 594-6473. To avoid any delay in the receipt of your accommodations, you should contact Student Disability Services as soon as possible. Please note that accommodations are not retroactive, and that accommodations based upon disability cannot be provided until you have presented your instructor with an accommodation letter from Student Disability Services. Your cooperation is appreciated.

5. OFFICE HOURS: MWF 11-noon in E410. Other times by prior arrangement.
GRADING POLICY A grade sheet containing all recorded grades will be posted in the glass case next to E406.

HOMEWORK & ATTENDANCE. Key study problems will be regularly assigned and selected problems will be discussed in class. Detailed homework solutions will be available for downloading by visiting the Blackboard electronic course reserve (https://blackboard.sdsu.edu/). Students should faithfully attend class and do all the assigned problems if they want to pass this very demanding course! Collaboration is encouraged but not copying of someone else’s work.

QUIZZES (8%). Several (4-5) surprise quizzes based on the relevant homework problems or assigned reading will be given on the day that a homework assignment is due.

SPICE DESIGN REPORTS (37%). Four written reports of your integrated circuit amplifier design will be required in this course. A penalty of 10% per day will apply to design reports submitted late. Design reports must be typed and placed in a folder with names of all the team members on the cover page. Additional details will be forthcoming.

ORAL PROGRESS REPORT (5%). On the day that a progress report is due, one of the team members will give a formal 5-7 minute oral presentation of their team’s design strategy and accomplishments.

MIDTERM (20%). Around the 8-9th week of the semester, there will be a non-comprehensive examination based on the study problems (listed below) and the design project completed up to that time.

FINAL EXAMINATION (30%). A two hour comprehensive examination will be given as per the schedule of classes. See date and time below.

FINAL COURSE GRADES will be determined using the above weighing factors. For quizzes, the midterm, and final, T-scores will be used. T-scores reflect a student’s performance on a graded item in relation to the whole class by combining the class average (X) and the standard deviation for that graded item (S) with the student’s own grade (x) using the following formula:

\[ T\text{-score} = \frac{(x-X)}{S} \times 10 + 50 \text{ so a T-score of 50 means average} \]

COURSE OUTLINE & HOMEWORK ASSIGNMENTS

Chap 1 - Models of Integrated Circuit Active Devices. [3 lectures] - HW prob. #3, 11-14, 16, 22
Chap 3 - Single and Two Transistor Amplifiers. [3 lectures] - HW prob. # 6, 10, 12, 13, 15, 21-23, 26
Chap 4 - Transistor Current Sources & Active Loads. [4 lectures] - HW prob. # 2, 3, 9, 13, 16, 25, 26, 38
Chap 2 - Bipolar, MOS, and BiCMOS IC Technology. [3 lectures] - HW prob. # 4, 12, 19, 20
Chap 5 - Output Stages. [2 lectures] - HW problems # 1a-b-c, 4, 5, 10, 11, 14-15, 17, 21

MIDTERM COVERING CHAPTERS 1-4 (TBA)

Chap 6 - Operational Amplifiers. [6 lectures] - HW problems # 3, 6, 11a-b-d-c, 15, 18, 25, 28, 27, 29
Chap 7 - Frequency Response of ICs. [5 lectures] - HW problems # 2, 6, 8, 15, 21, 27, 30, 35
Chap 8 - Feedback. [4 lectures] - HW problems # 7, 11-13, 15, 20
Chap 9 - Frequency Response and Stability of Feedback Amplifiers [5 lectures] - HW problems # 2, 4, 6, 10, 20, 28
Chap 10 & 11 - Nonlinear Analog Circuits and Noise in ICs. [2 lectures] (if time permits) -
Design Projects - Oral Reports on days that the design reports are due. [4 lectures]

FINAL EXAMINATION on the last day of lecture, May 4, 2016.